BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Huang, et al. Application No.: 10/727,319 Filed: 12/3/2003 Title: METHOD AND SYSTEM FOR POWER MANAGEMENT INCLUDING DEVICE CONTROLLER-BASED DEVICE USE EVALUATION AND POWER-STATE CONTROL Attorney Docket No.: AUS920030761US1	Art Unit: 2116 Examiner: SUGENT, JAMES F.

Mail Stop - Appeal Brief
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APPEAL BRIEF

Dear Sir:

This brief is submitted in support of the Appeal in the above-identified application. The requisite fee of $500 has been paid at electronic filing of this Appeal Brief.

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REAL PARTY IN INTEREST

The present application is assigned to International Business Machines Corporation, the real party in interest.

RELATED APPEALS AND INTERFERENCES

No related action is presently pending.

STATUS OF CLAIMS

Claims 1, 3-11, 13-15 and 18-20 stand finally rejected by the Examiner as noted in the Final Office Action dated August 28, 2006. Claims 2, 12 and 16-17 were previously canceled. Appellants appeal from all of the rejections of Claims 1, 3-11, 13-15 and 18-20.

STATUS OF AMENDMENTS

No Amendment was filed in response to the Final Office Action dated August 28,2006.

SUMMARY OF CLAIMED SUBJECT MATTER

The invention as recited in independent Claims 1 and 10 and 15 encompasses a device controller (Claim 1) processing system (Claim 10) in which device usage is measured by usage evaluators. In the embodiment depicted in Figure 2 and described in the

Specification at pg. 14, line 12 through pg. 15, line 5, the usage evaluators are inter-arrival time evaluators 25A-25D.

The device controller and processing system provide that the state of the usage evaluator can be retrieved and stored externally to the device controller via an output port and restored via an input port. Such an input and output port is provided by I/O interface 27 of Figure 2 and Figure 3 and are described in the Specification at pg. 14, line 12 through pg. 15, line 20.

A method (Claim 15), which is depicted in an embodiment in the flowchart of Figure 4 and described in the Specification at pg. 16, lines 12-29, stores the state of the usage evaluator, which are memory access inter-arrival time counters in the depicted embodiment, when a process is deactivated and restores the stored state when the process is subsequently re-activated, so that the usage evaluation commences from the previously stored state.

None of the Claims include means-plus-function or step-plus-function limitations under 35 U.S.C. §112,¶6.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The Examiner has rejected Claims 1, 3-11, 13 and 14 under 35 U.S.C. §102(b) as being anticipated by Faucher, et al. (U.S.

5,404,543). The Examiner has rejected Claims 15 and 18-20 under 35 U.S.C. §103(a) as being unpatentable over Faucher in view of Fleck, et al. (U.S. 6,128,641). The Examiner has provisionally rejected Claims 1, 3, 10 and 11 on the ground of obviousness-type double-patenting as being unpatentable over Claims 8-10 of co-pending U.S. Patent Application 10/727,320 in view of Faucher.

ARGUMENT

The Examiner's rejections of Claims 1, 3-11, 13-15 and 18-20 are not well-founded and should be reversed.

I. *Faucher* does not disclose the invention of Claims 1, 3-11, 13 and 14.

Independent Claim 1 (and similarly independent Claim 10) recites:

> "A device controller for coupling one or more controlled devices to one or more processors in a processing system, comprising:
> a command unit for sending commands to said one or more devices;
> at least one usage evaluator having an input coupled to an output of said command unit for evaluating a frequency of use of an associated controlled device;
> control logic coupled to said usage evaluator and further coupled to an input of said command unit for sending power management commands in response to said usage evaluator detecting that a usage level of said associated device has fallen below a threshold level, whereby said device controller power manages said

controlled device without intervention by said one or more processors;

an output port coupled to said at least one usage evaluator **for reading a state of said at least one usage evaluator, whereby a state of said at least one usage evaluator may be stored external to said device controller;** and

an input port coupled to said at least one usage evaluator **for setting a state of said at least one usage evaluator, whereby said state of said at least one usage evaluator may be restored from information stored external to said device controller."** [bold text added for emphasis]

Faucher does not disclose an output port and input port for reading and setting a state of the usage evaluator so that the state can be stored and restored external to the device controller.

The structure described in Faucher does not enable preservation of such usage evaluator state information and Faucher does not describe any such action nor include an input and output port that enable such action with respect to the state of the usage evaluators.

In particular, in the Final Office Action, the Examiner expresses the belief that the power management machine 66 in Figure 3 of Faucher, and on which the Examiner reads the usage evaluator of the Claims, includes an output port that sends data to programmable memory power system 24 in Figures 1-2 of Faucher that may be stored external to the memory controller. The Examiner also expressed the belief that the usage evaluator

(which the Examiner reads onto power management machine 66 of Faucher) includes an input port by which the state of the usage evaluator may be restored.

Faucher discloses only two types of buses connected between programmable memory power system 24 and power management machine 66. See Faucher, Figure 2. The first bus are control buses 36, and the second type is the voltage programmable bus 46. Control buses 36 carry signals that indicate the memory bank to which the data on voltage programmable bus 46 applies. See Faucher, col. 4, lines 60-63. Voltage programmable bus 46 digitally encodes the voltage applied to each memory bank and provides the digital representation of the voltage to programmable memory power system 24. See Faucher, col. 4, line 58 through col. 5, line 5.

The encoded voltage is *selected in response to* a usage evaluation, which is a determination of whether or not a bank has been accessed since the last diagnostic completion. See Faucher at col. 9, line 56 through col. 10, line 48. However, the selected voltage is not the "state" of the usage evaluator itself in the context of the present invention, but is rather the result of a decision-making process that is driven by a determination of whether or not a particular memory bank has been used since a last diagnostic check. See Id.

In the present invention, the state of a usage evaluation can be preserved, via the input and output ports, for each thread across thread execution slices and is described in the exemplary embodiment as the state of the inter-arrival counts and/or statistics of usage evaluators 25A-D. See the Specification at page 14, lines 25-32.

Faucher does not restore any usage evaluator state via an input port, and if the usage evaluator state were taken as the above digital memory voltage representation that is "stored" in programmable memory power system 24, then there is no mechanism disclosed in Faucher to restore those values from programmable memory power system 24 to memory controller 20.

In the Final Office Action, the input port of Faucher cited by the Examiner was indicated as "an input port at which the usage evaluator receives data from outside of the memory controller from memory banks." However, Faucher discloses that the information retrieved from the memory banks is merely configuration information, and appears to be the configuration information as well-known in the art to be typically supplied to a memory controller by a configuration bus (presence bus). The configuration information includes data regarding what banks are present, memory size, addressing, timing characteristics, which are simply the hard-wired characteristics of the particular

memory devices installed in the system that are provided for automatic system configuration and have nothing to do with usage evaluation. See Faucher at col. 4, lines 41-47.

Therefore, the state retrieved by memory controller 20 from system memory 22 not only *is not* the state of usage evaluators, but further *is not identical* to the value the Examiner indicates as being the state of the usage evaluators in his analysis of Faucher with respect to the output port element of the Claims.

In the Advisory Action, the Examiner states that the disclosure of Faucher "necessitates the input power being coupled to the evaluator via the scoreboard" and cites passages describing information stored within the scoreboard. However, assuming *arguendo* that the Faucher does store usage evaluator state information via an output port, since the state information *would be* provided to the power management machine 66 of Faucher from memory controller 20 via the "output port" (which the Examiner reads onto control bus 36 and programmable voltage bus 46 of Faucher), there is no necessity to retrieve such state information from the power management machine, as it is already present in memory controller 20. The Examiner is using the disclosure of the types of information stored within the "scoreboard" of memory controller 20 as shown in Figure 4 of

Faucher in attempt to support his assumption that all of the values are read to and written from an external storage.

Finally, the buses referred to by the Examiner as disclosing the storing and restoring of the input and output port elements of the Claims, do not connect to the same blocks in Faucher. As described above and as shown in Figure 2 of Faucher, the control bus 36 and programmable voltage bus 46 connect the memory controller 20 and programmable memory system 24 of Faucher, while the bidirectional memory data bus 34, presence detect bus 40 and "information provided to the memory controller" 44, as cited in the Advisory action, connect system memory 22 to memory controller 20. The only outputs of programmable memory system 24 as shown in Figure 2 of Faucher are 48 voltage signals that are subsequently de-glitched by deglitch circuits 50 to provide the actual voltage signals to the corresponding memory banks 30. See Faucher col. 4, line 67 through col. 5, line 12, which describes programmable memory power system 24 as including DC/DC regulators that supply the voltage signals 48, and are therefore not the state of a usage evaluator.

Therefore, even if power management machine 66 contained usage evaluator(s) as asserted by the Examiner in the Final Office Action, there is no disclosed mechanism in the depicted embodiment of Faucher to support storing a state of the usage

evaluator(s) in external storage and restoring that state from external storage.

Therefore, the Examiner's rejection of Claims 1, 3-11, 13 and 14 under 35 U.S.C. §102(b) as being anticipated by Faucher is not well founded.

II. *Faucher* in view of *Fleck* does not disclose or suggest the invention of Claims 15 and 18-20.

The Examiner has rejected Claims 15 and 18-20 under 35 U.S.C. §103(a) as being unpatentable over Faucher in view of Fleck, et al.(U.S. 6,128,641). Applicants respectfully disagree. For the reasons stated above, Faucher does not disclose the invention as recited in the independent Claims, and neither does the combination of Faucher and Fleck disclose or suggest the claimed invention. Fleck discloses only an apparatus and methodology for saving state information upon a thread context switch and does not disclose usage evaluators, nor a device controller having input and output ports for saving the state of the usage evaluators.

Therefore, the Examiner's rejection of Claims 15 and 18-20 under 35 U.S.C. §103(a) as being unpatentable over Faucher in view of Fleck is not well founded.

III. *Faucher* does not make obvious Claims 1, 3, 10 and 11 in view of the invention recited in Claims 8-10 of co-pending U.S. Patent Application 10/727,320.

The Examiner has provisionally rejected Claims 1, 3, 10 and 11 on the ground of obviousness-type double-patenting as being unpatentable over Claims 8-10 of co-pending U.S. Patent Application 10/727,320 in view of Faucher. (The Double-Patenting rejection in the Final Office Action also relies on Claims 16 and 18-19 of U.S. Patent Application 10/727,320, which have been canceled.)

Claims 8-10 of U.S. Patent Application 10/727,320 are directed to a processor in which power management is performed according to a global power consumption bound by communicating local power bounds to multiple device controllers, which may be memory controllers as recited in Claim 9, and/or in which the device controllers include usage evaluators that determine whether a usage of a device has fallen below a threshold.

None of the Claims of U.S. Patent Application 10/727,320 include both the input and output ports for reading and setting the state of the usage evaluators as recited in all of the independent claims of the present application.

The Examiner indicated in the Final Office Action, that Faucher discloses such input and output ports and therefore makes Claims 1, 3, 10 and 11 of the present application obvious in light of U.S. Patent Application 10/727,320. However, for the same reasons argued above with respect to the rejection under 35 U.S.C. §102, Faucher does not disclose or suggest the input and output ports for saving and restoring the state of usage evaluators as recited in the Claims.

Therefore Applicants believe that the provisional obviousness-type double-patenting rejection is not well founded.

CONCLUSION

For the reasons stated above, Appellants believe that the claimed invention clearly is patentably distinct over the cited references and that the rejections under 35 U.S.C. §103(a) are not well-founded. Hence, Appellants respectfully urge the Board to reverse the Examiner's rejections.

The fees for the Notice of Appeal and for submission of a Brief in Support of Appeal have been paid. No additional fee or extension of time is believed to be required; however, in the event an additional fee or extension of time is required, please charge that fee or extension of time requested to IBM Deposit Account 09-0447.

Respectfully Submitted,

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CLAIMS APPENDIX

1. A device controller for coupling one or more controlled devices to one or more processors in a processing system, comprising:

a command unit for sending commands to said one or more devices;

at least one usage evaluator having an input coupled to an output of said command unit for evaluating a frequency of use of an associated controlled device;

control logic coupled to said usage evaluator and further coupled to an input of said command unit for sending power management commands in response to said usage evaluator detecting that a usage level of said associated device has fallen below a threshold level, whereby said device controller power manages said controlled device without intervention by said one or more processors;

an output port coupled to said at least one usage evaluator for reading a state of said at least one usage evaluator, whereby a state of said at least one usage evaluator may be stored external to said device controller; and

an input port coupled to said at least one usage evaluator for setting a state of said at least one usage evaluator, whereby

said state of said at least one usage evaluator may be restored from information stored external to said device controller.

3. The device controller of Claim 1, wherein said device controller is a memory controller, and wherein said controlled devices are memory modules.

4. The device controller of Claim 3, wherein said at least one usage evaluator comprises an inter-arrival time counter for determining an interval between accesses to said associated memory module.

5. The device controller of Claim 1, further comprising one or more power management control registers, each associated with a particular one of said one or more controlled devices, each coupled to said input port of said device controller and further coupled to said command unit, whereby a power management control state for said associated controlled device can be set by said one or more processors and set in said associated controlled device by said device controller.

6. The device controller of Claim 5, wherein said power management control registers are further coupled to said at least

one usage evaluator, whereby values of said power management control registers are adjusted in conformity with a result of said evaluating.

7. The device controller of Claim 1, wherein said evaluator further comprises an adaptive threshold circuit for adjusting said threshold in response to said evaluated frequency of use of said one or more controlled devices.

8. The device controller of Claim 1, wherein said one or more controlled devices include a counter for determining a level of usage of each controlled device during a current process, and wherein said device controller further comprises another input port coupled to each of said controlled devices for reading a value of said counter, and wherein said control logic updates said at associated evaluator in conformity with said value of said counter.

9. The device controller of Claim 8, wherein said device controller is a memory controller, wherein said controlled devices are memory modules incorporating usage counters, and wherein said control logic is coupled to said command logic

whereby said control logic periodically reads current counts from said memory modules.

10. A processing system, comprising:

a processor;

a memory coupled to said processor for storing program instructions and data values;

a device controller coupled to said processor;

one or more controlled devices coupled to said device controller, wherein said controlled devices have multiple power management states, and wherein said device controller includes a command unit for sending commands to said one or more devices, at least one usage evaluator having an input coupled to an output of said command unit for evaluating a frequency of use of an associated controlled device, and control logic coupled to said usage evaluator and further coupled to an input of said command unit for sending power management commands in response to said usage evaluator detecting that a usage level of said associated device has fallen below a threshold level, whereby said device controller power manages said controlled device without intervention by said processor, and wherein said device controller further includes an output port coupled to said at least one usage evaluator for reading a state of said at least

one usage evaluator by said processor, whereby a state of said at least one usage evaluator may be stored in said memory by said processor, and an input port coupled to said at least one usage evaluator for setting a state of said at least one usage evaluator by said processor, whereby said state of said at least one usage evaluator may be restored from said memory.

11. The processing system of Claim 10, wherein said device controller is a memory controller, and wherein said controlled devices are memory modules.

13. The processing system of Claim 10, wherein said at least one usage evaluator comprises an inter-arrival time counter for determining an interval between commands sent to said associated controlled device.

14. The processing system of Claim 10, wherein said device controller further comprises one or more power management control registers, each associated with a particular one of said one or more controlled devices, each coupled to said input port of said device controller and further coupled to said command unit, whereby a power management control state for said associated

controlled device can be set by said processor and set in said associated controlled device by said device controller.

15. A method of managing power in a processing system, comprising:

sending power management setting information for devices controlled by a device controller to said device controller;

evaluating a usage of each of said controlled devices within said device controller in order to determine whether or not said usage has fallen below a threshold;

sending power management commands from said device controller to said controlled devices in conformity with a result of said determining, whereby said device controller manages a power management state of said controlled devices without processor intervention;

receiving an indication of a context switch activating a second process and deactivating a first process; and

in response to said receiving, saving a state of said evaluating;

second receiving a second indication of a second context switch reactivating said first process; and

in response to said second receiving, restoring said saved state of said evaluating, whereby said evaluating commences from the previously stored state.

18. The method of Claim 15, further comprising retrieving usage counts from said controlled devices, and wherein said evaluating is performed in conformity with said retrieved usage counts.

19. The method of Claim 15, further comprising adjusting said threshold in accordance with a result of said evaluating, whereby said evaluating is made adaptive to said usage.

20. The method of Claim 15, wherein said device controller is a memory controller, wherein said controlled devices are memory modules, wherein said sending sends power management setting information to said memory modules, and wherein said evaluating determines a frequency of accesses to said memory modules.

RELATED APPEALS AND INTERFERENCES APPENDIX

none

EVIDENCE APPENDIX

none